



Reliability Test Station

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Engineering



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Overview

- Motivation
- System Specifications & Features
- UF Semiconductor Reliability System
- Implementation & Development
- Data
- AFRL HEMT status

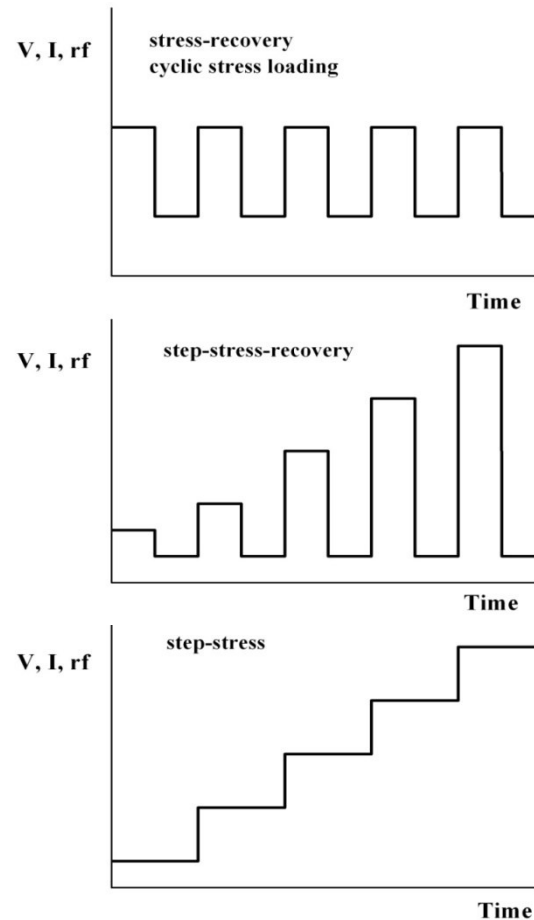
Motivation

	Turnkey		In-house
Timeline	Purchase lead time		On-going
System	Proven		Custom design
Objective	Determine Lifetimes		Research Determine failure mechanisms
Test Types	Industry standards		Flexible
DC Drain Gate	0-100V, up to 4A, 400W max ±18.5V, up to 200mA		0-60V, up to 6A, 300W max ±10V, up to 20mA
RF	600MHz-3 GHz 2-18 GHz 58-60 GHz	900MHz-10GHz 36-40 GHz 76-78 GHz	1.8-2.2 GHz expandable with additional hardware
Temperature	50° to 250° C		25° to 200° C
Optical	NA		Research with wavelength and intensity
Thermal Imaging	NA		IR, Micro Raman additional hardware
Pulse	1-100kHz		1-1MHz+
Data Storage	Independent test files		SQL database

System Specifications & Features

- 16 Device Capacity
 - Individual device control
 - Gate bias
 - ±10Vdc up to 20mA
 - Drain bias
 - 0-60Vdc, 6A max, 300W max
 - Over-current & over-voltage protection
 - Temperature
 - 25-200° C Peltier heating
 - PID control
 - Grouped into 4

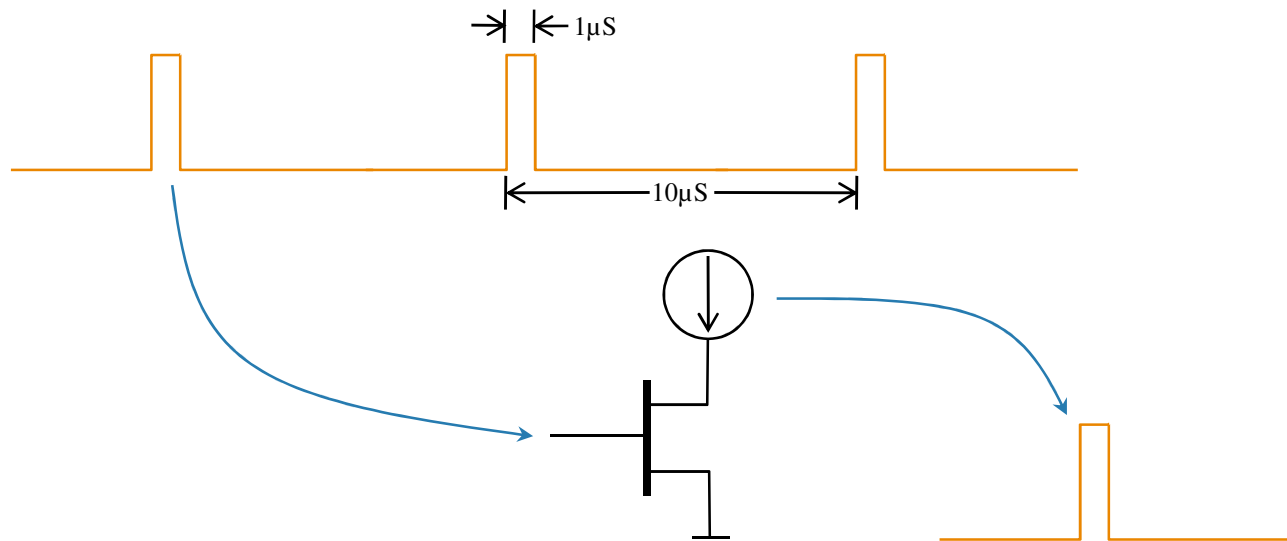
System Specifications & Features



- Long-term DC Stress
 - Types
 - Stress-recovery
 - Step-stress-recovery
 - Step-stress
 - Device Characteristics
 - IV curve
 - Transconductance, V_T
- RF Stress
 - 2 GHz

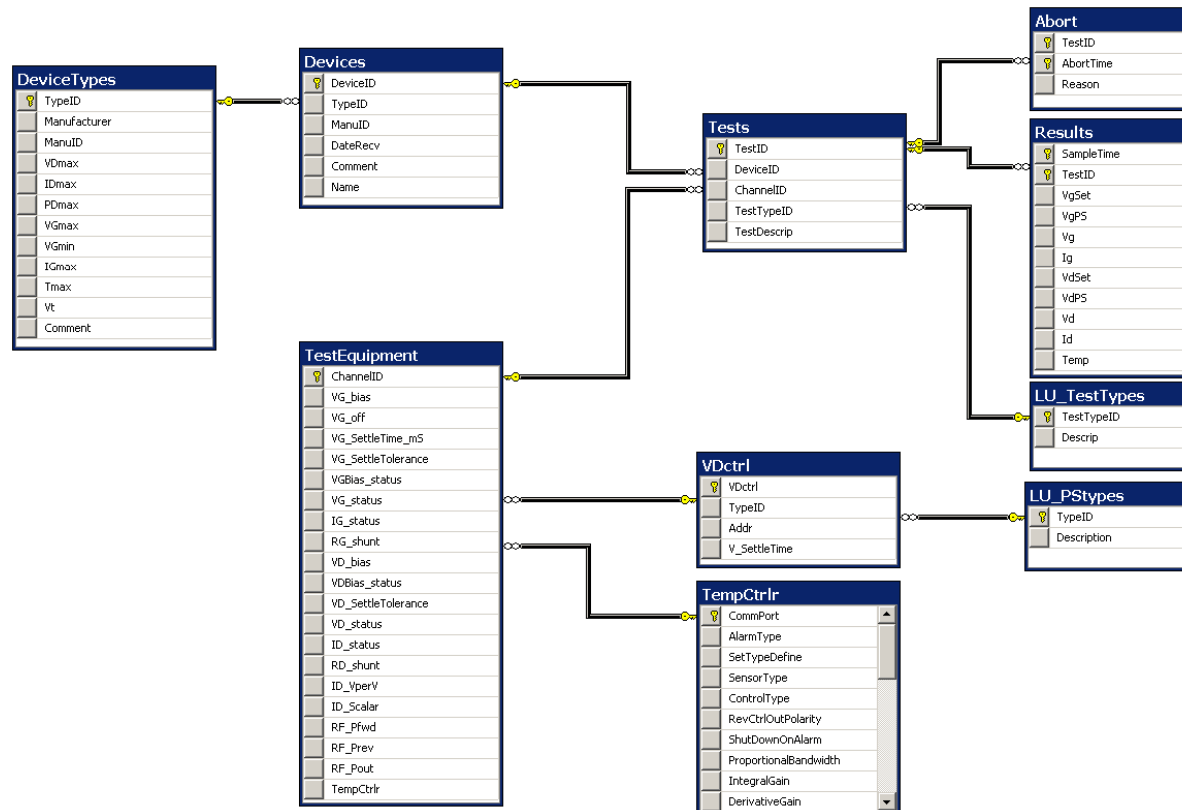
System Specifications & Features

- Gate Pulse Tests
 - High-speed 100kHz @ 10% duty cycle
 - Indicator of surface traps
 - Apply to gate V_g and measure I_d response



System Specifications & Features

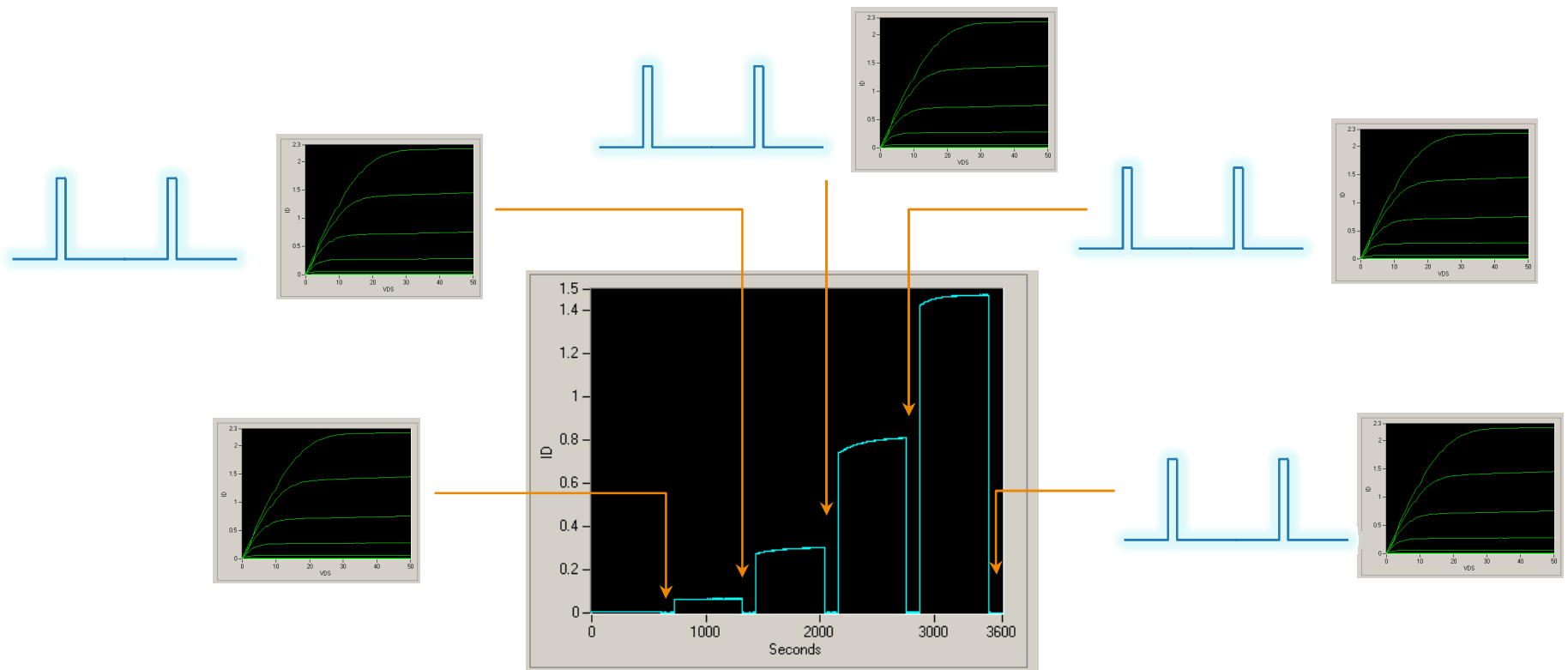
- Data Storage
 - One second sample
 - SQL Server: Design flexibility, Data queries



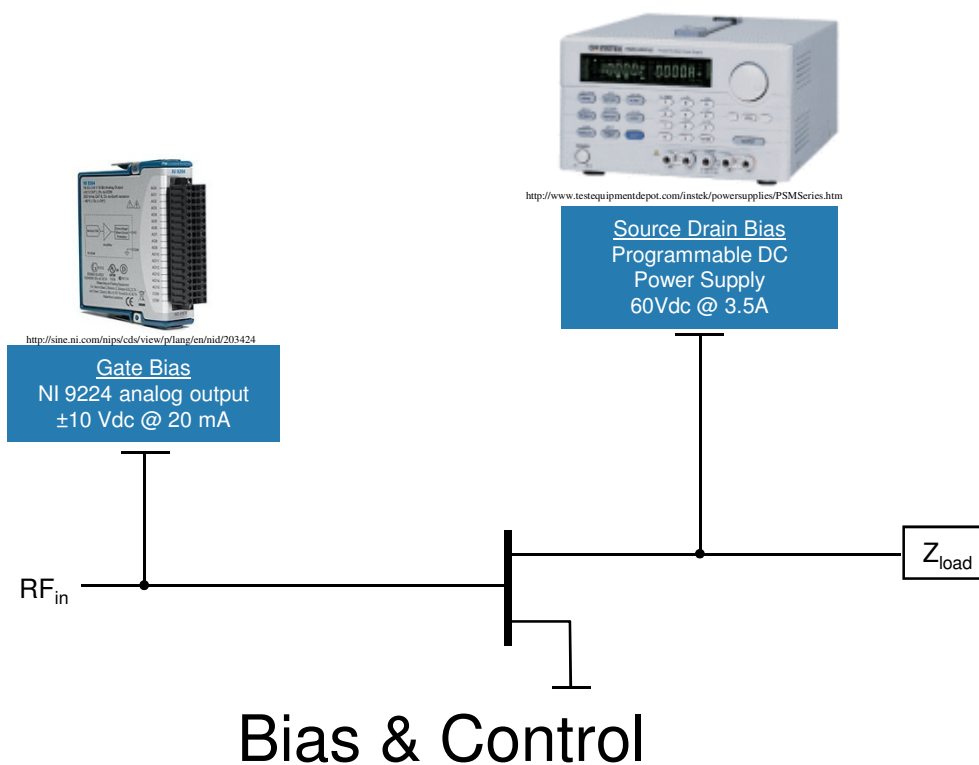
System Specifications & Features

■ Sequencing

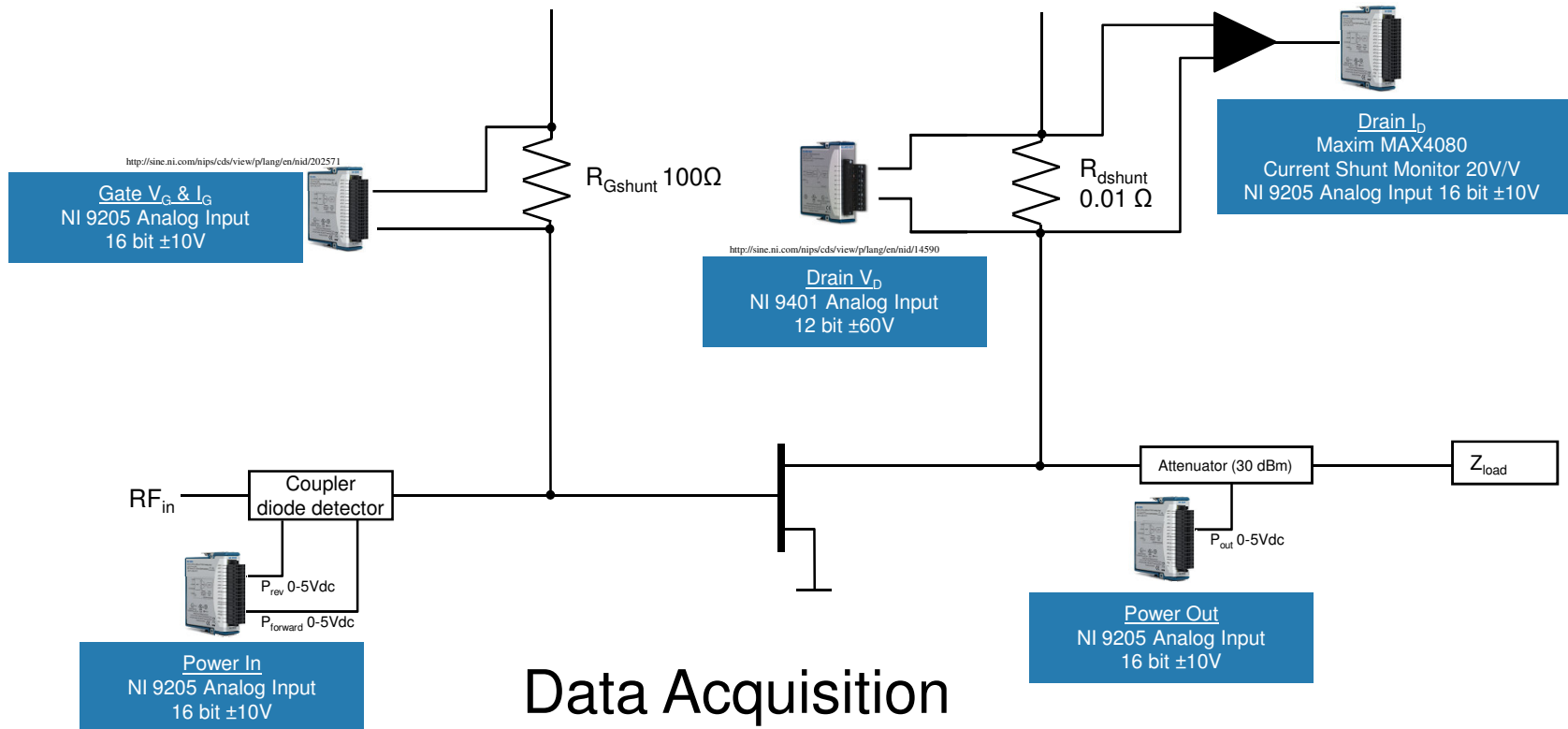
- IV curve \Rightarrow DC Stress \Rightarrow Pulse \Rightarrow IV curve \Rightarrow DC Stress ...
- Pile plot IV curves



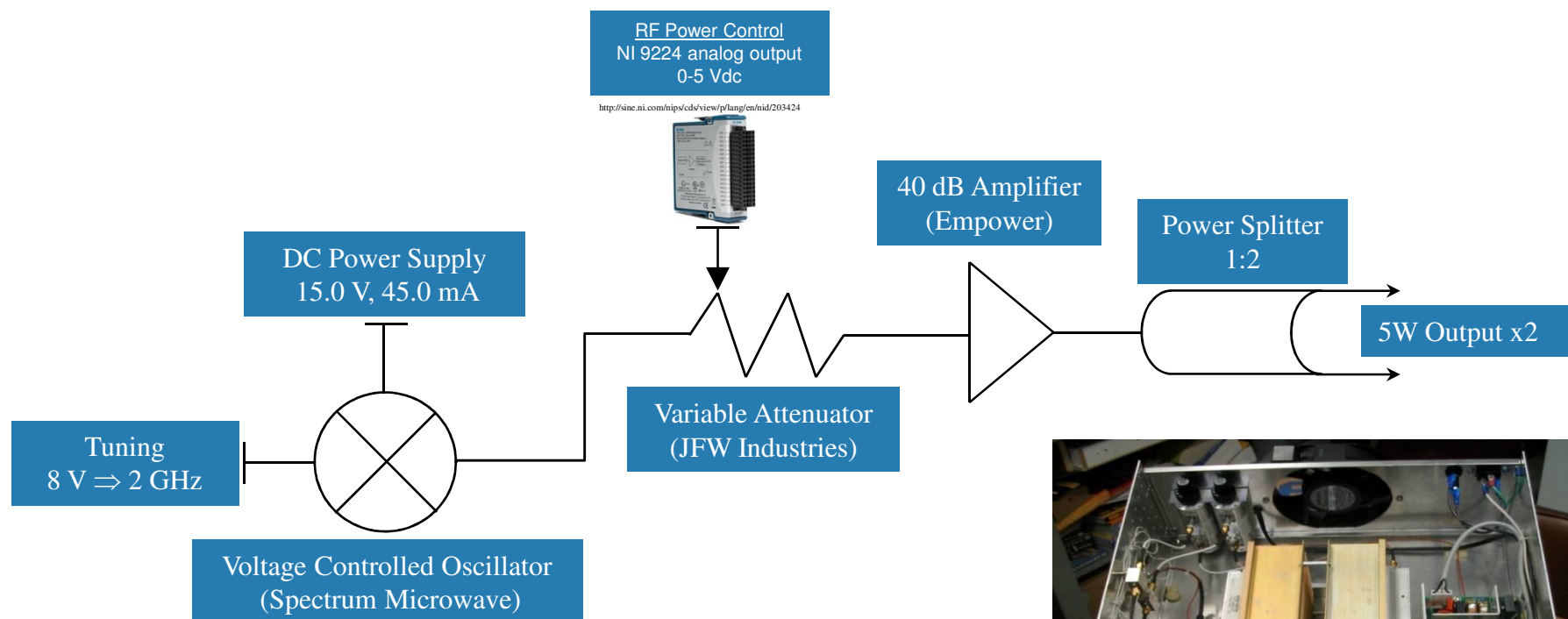
UF Semiconductor Reliability System



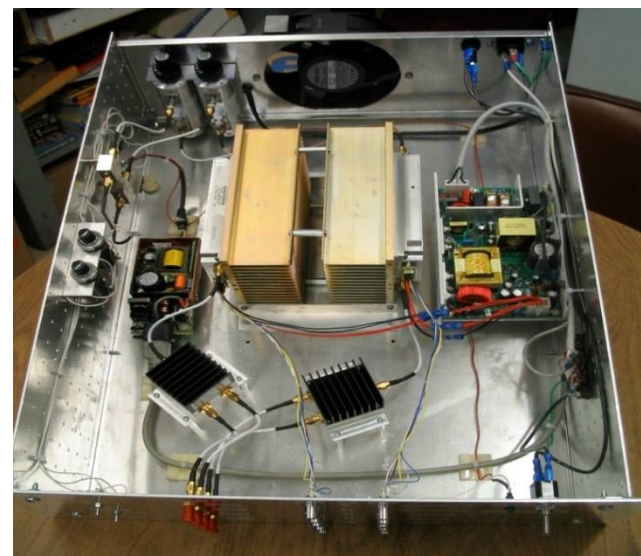
UF Semiconductor Reliability System



UF Semiconductor Reliability System



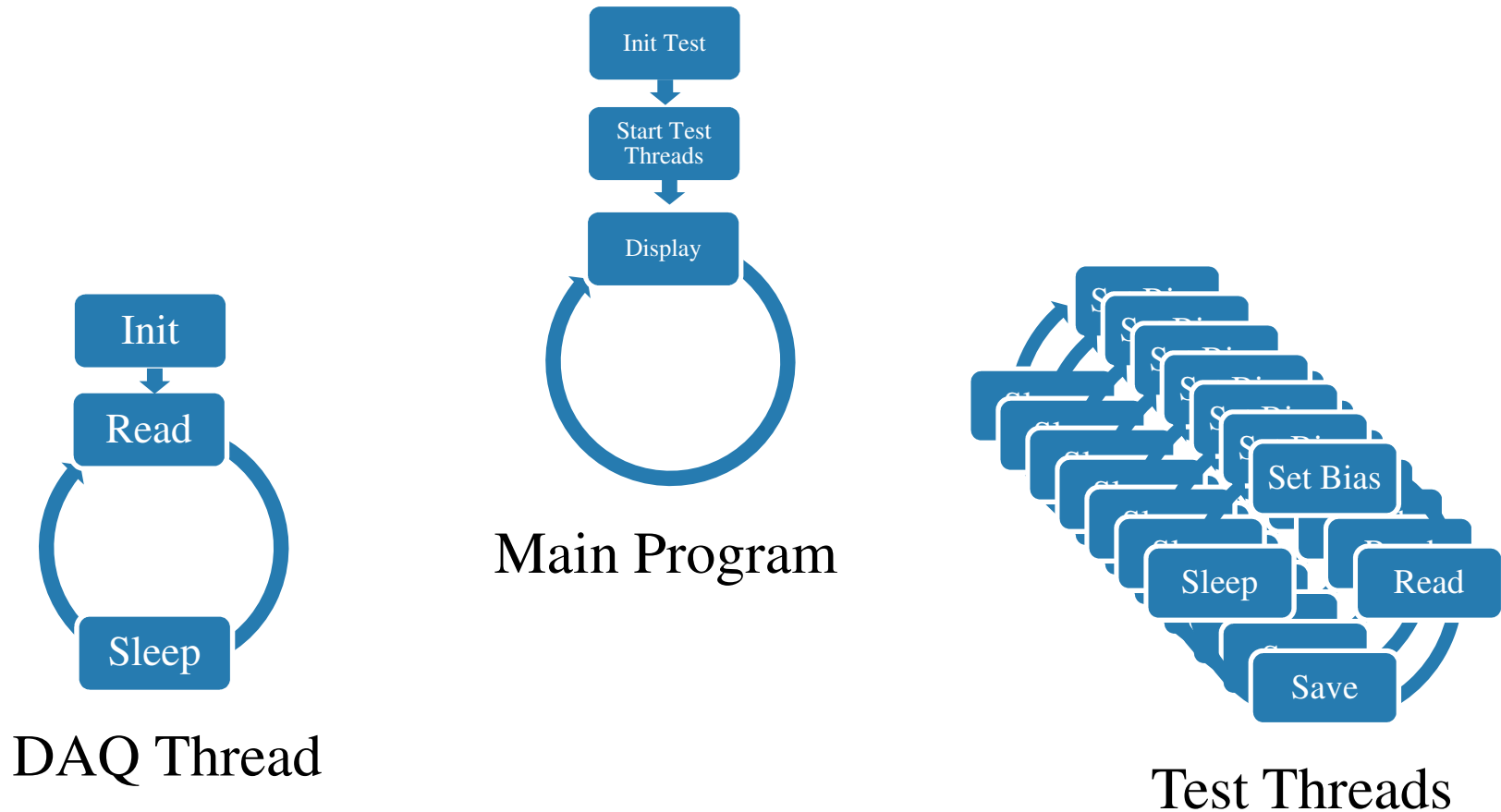
RF Power Supply (x4)



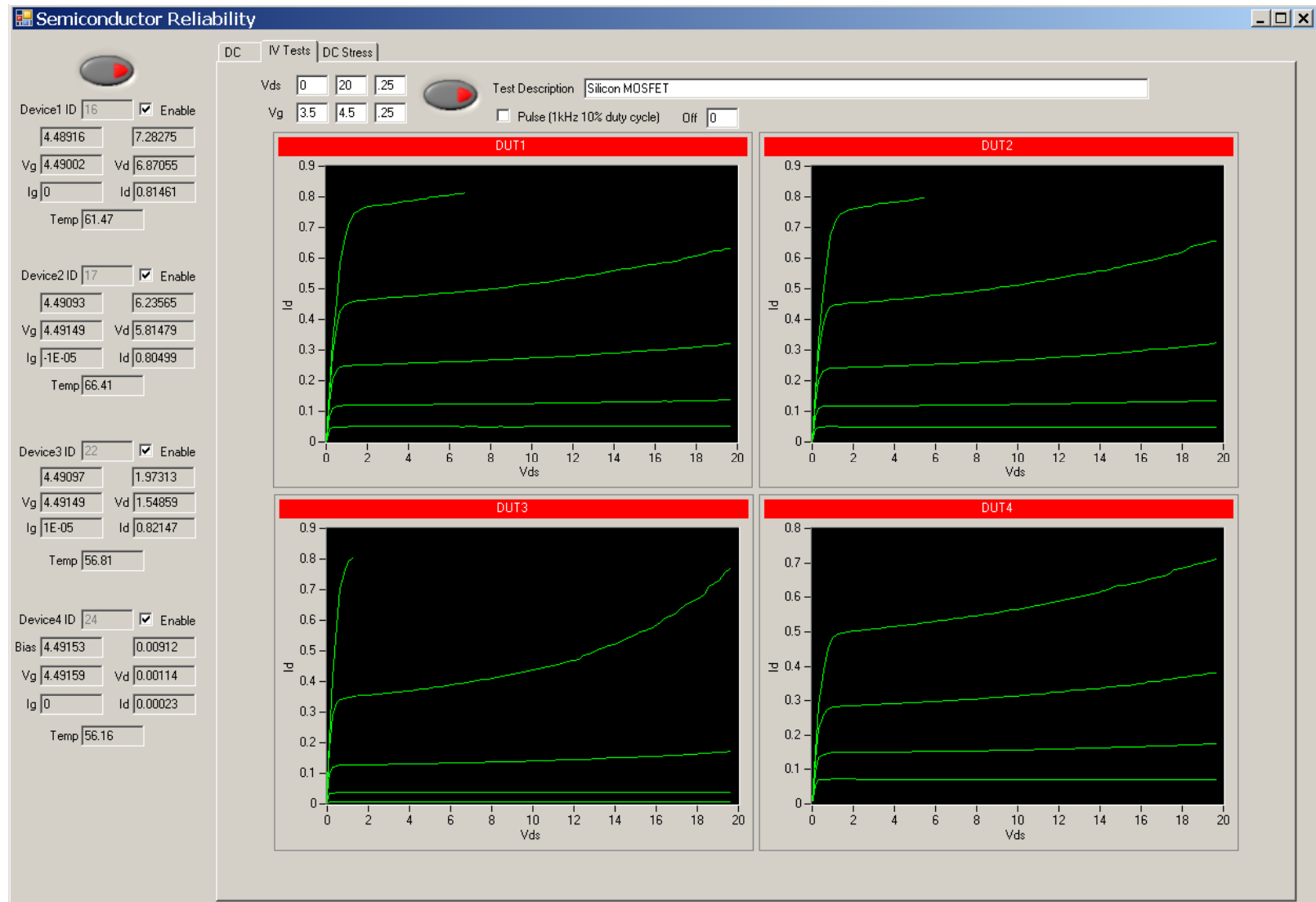
Implementation & Development

- ✓ Single Device Test: IV or DC
- ✓ Multiple Device Testing
 - ✓ Multi-threaded four devices
 - ✓ Scalable to 16
- ✓ Pulse Test
 - ✓ 1-2kHz – All channels
 - ◎ 1-80kHz – 8 channels
 - 1-1MHz+ – 4 channels
- ✓ Sequencing
 - ✓ Hardcoded: IV-DC-IV-DC.... 5 levels
 - Flexible: user-defined
- RF Testing
 - Out-source tuning expertise
- Optical pumping

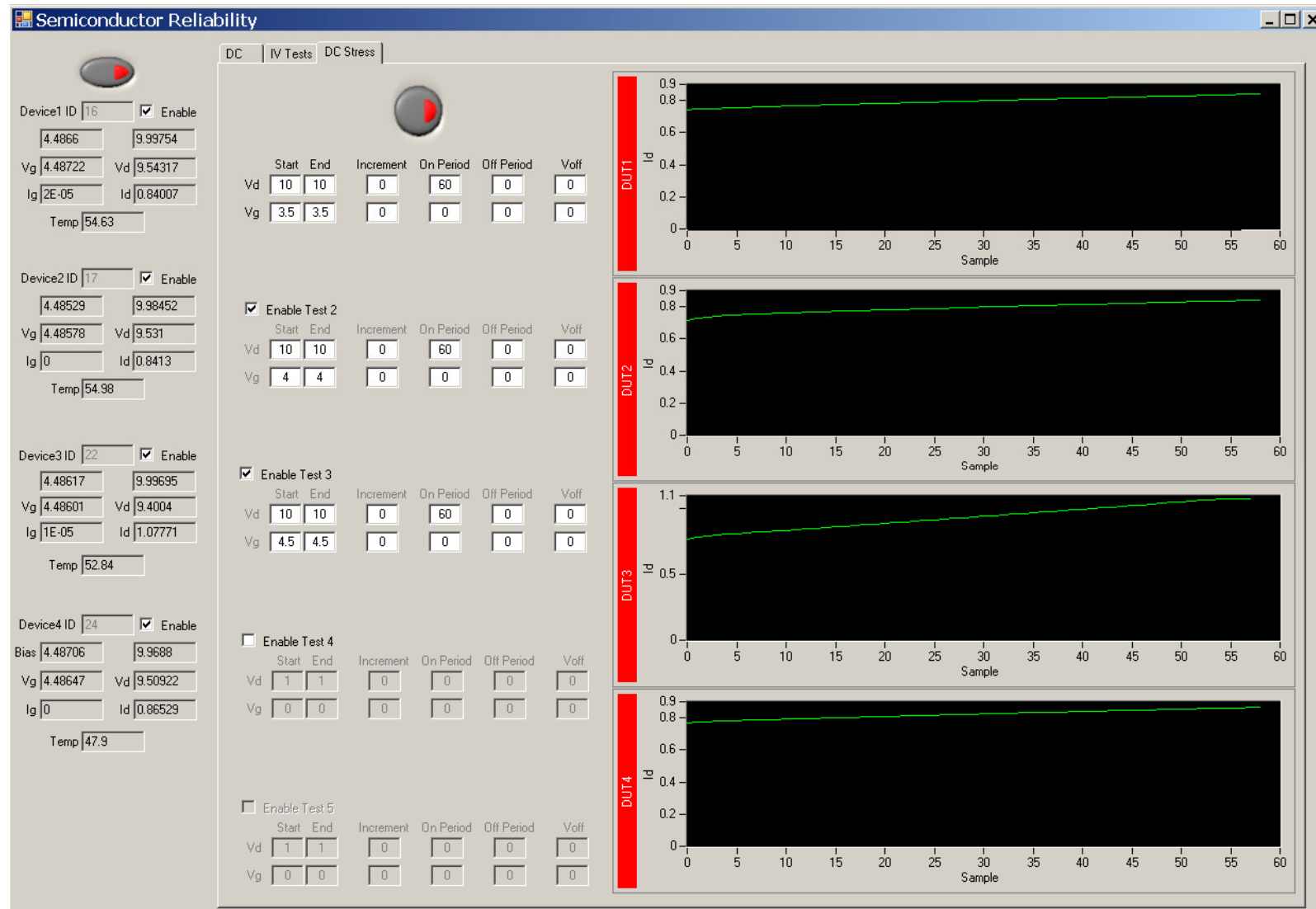
Implementation & Development



Implementation & Development

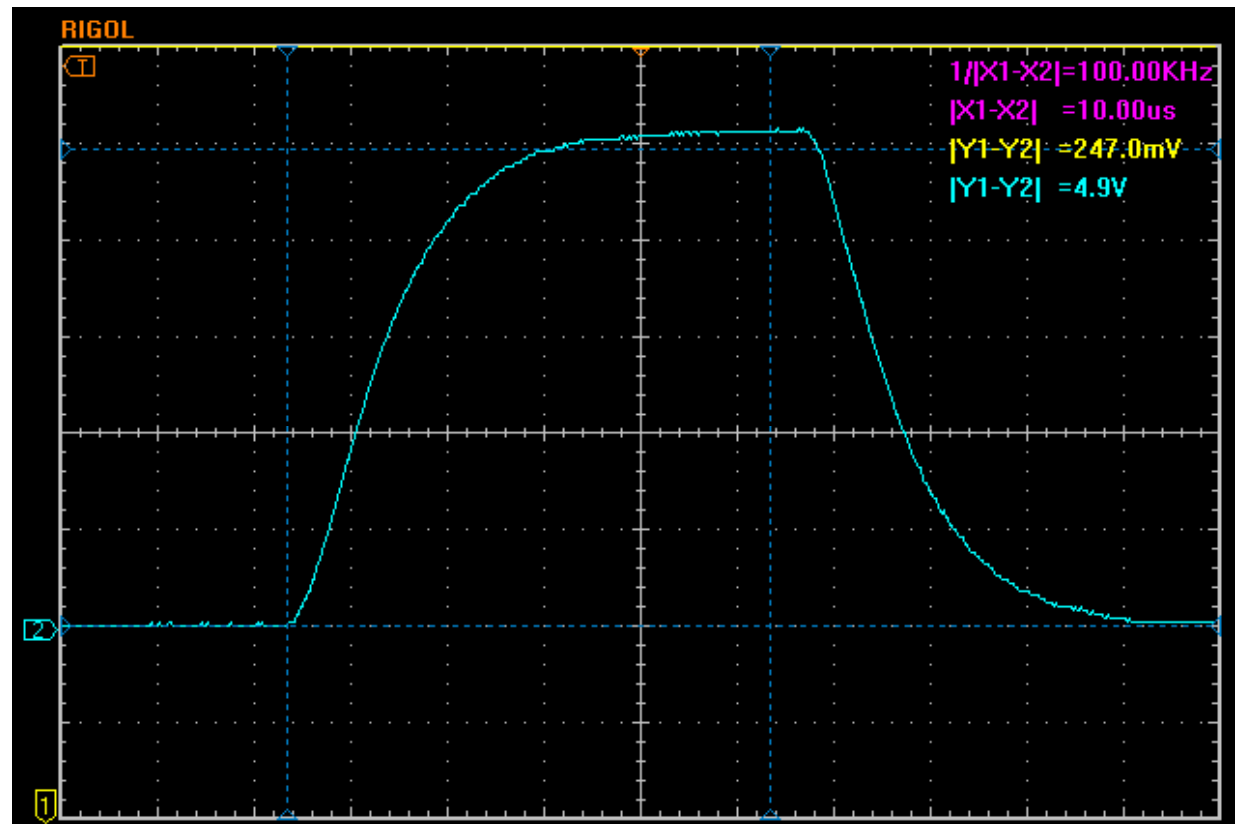


Implementation & Development



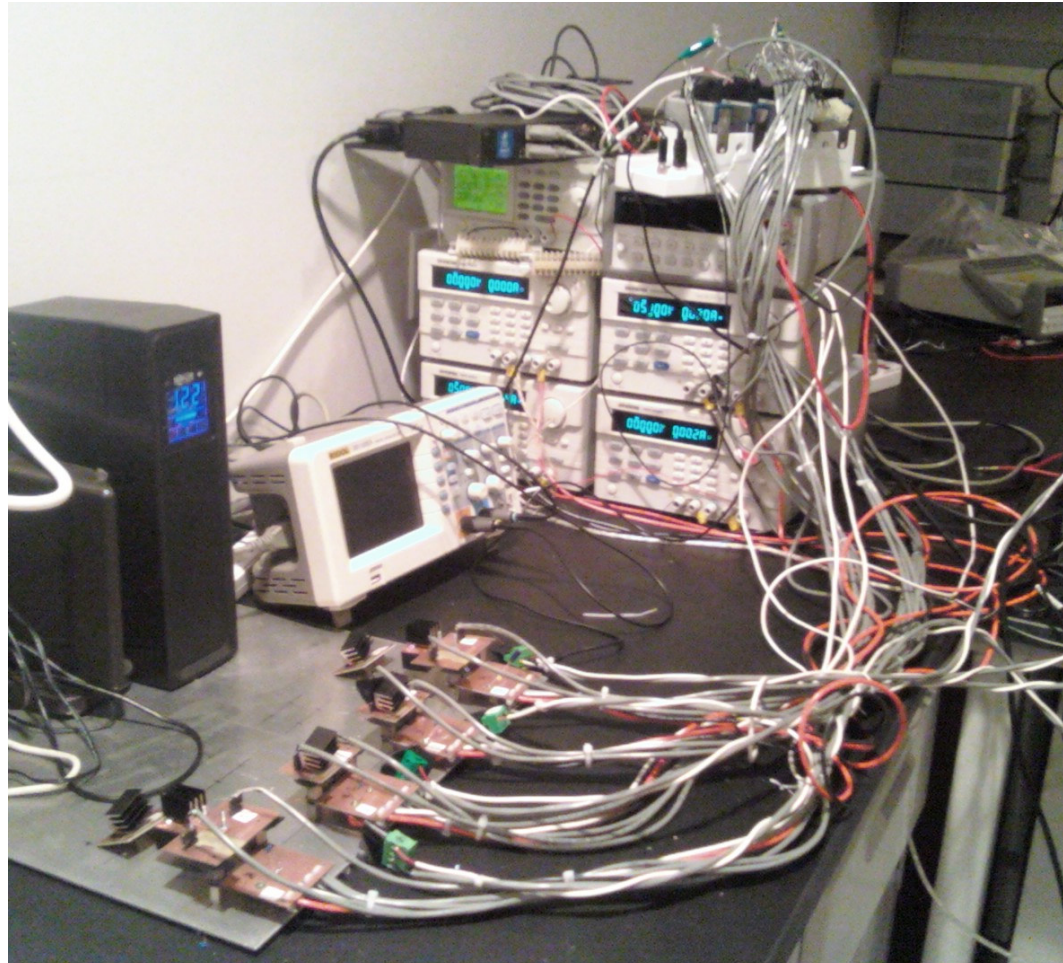
Implementation & Development

- Pulse Output
 - “Square enough”
 - 100 μ S, 10 μ S, 1 μ S
- Read
 - Coordination
 - Number of samples
 - Triggering



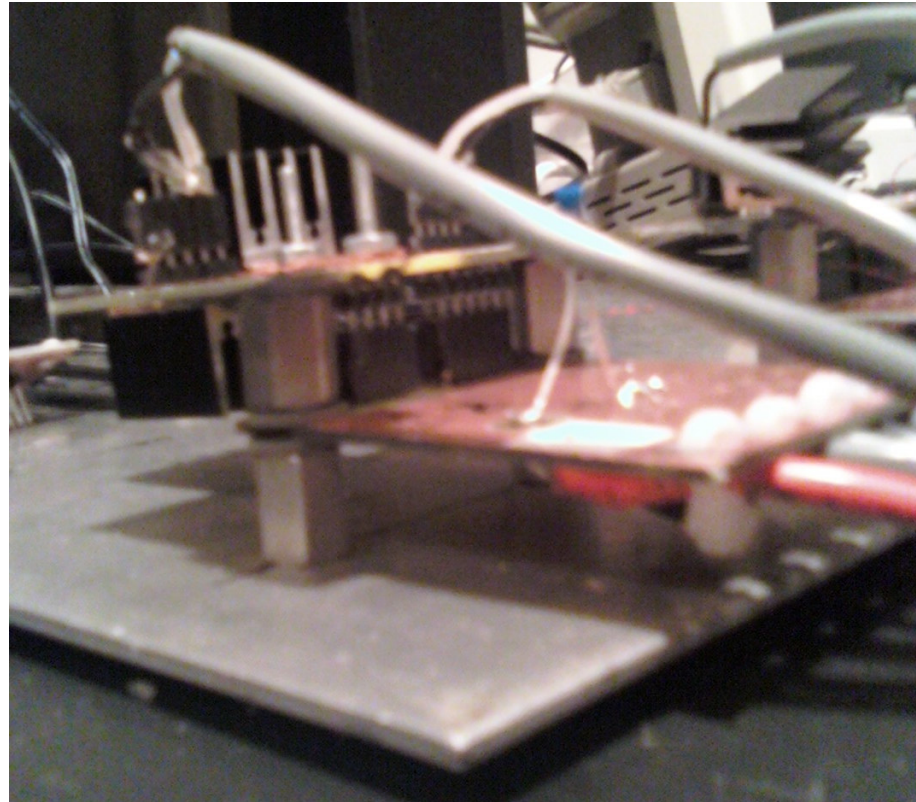
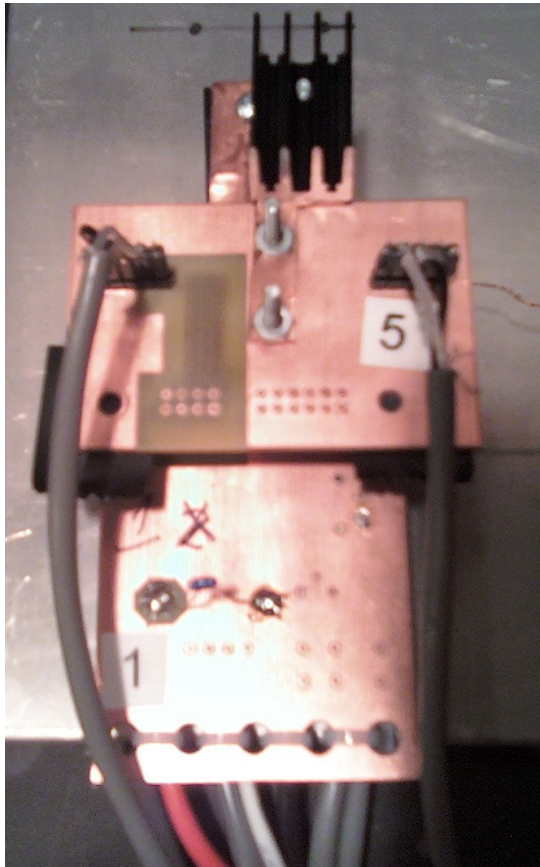
Implementation & Development

System During Development



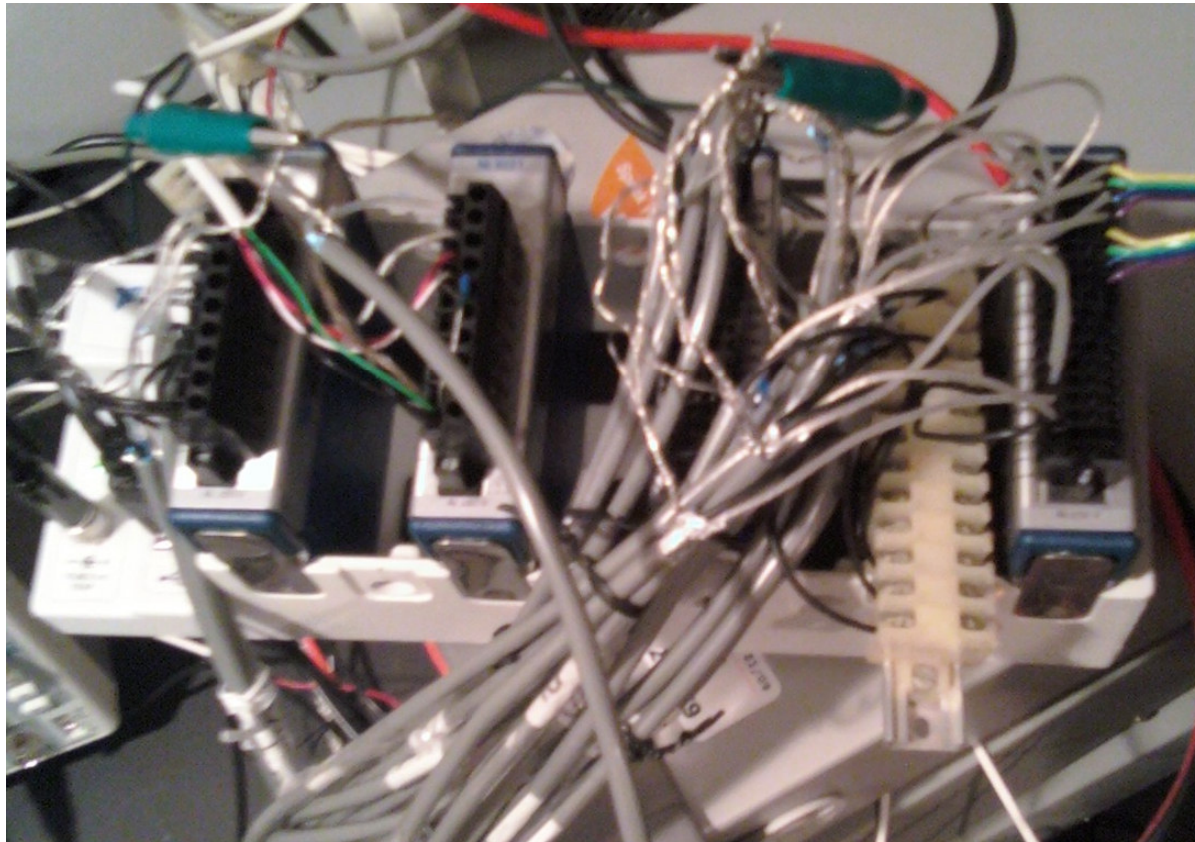
Implementation & Development

- Split board design
 - Sense resistors
 - Boards for each package



Implementation & Development

DAQ Equipment



Implementation & Development

Tower of Power



Implementation & Development

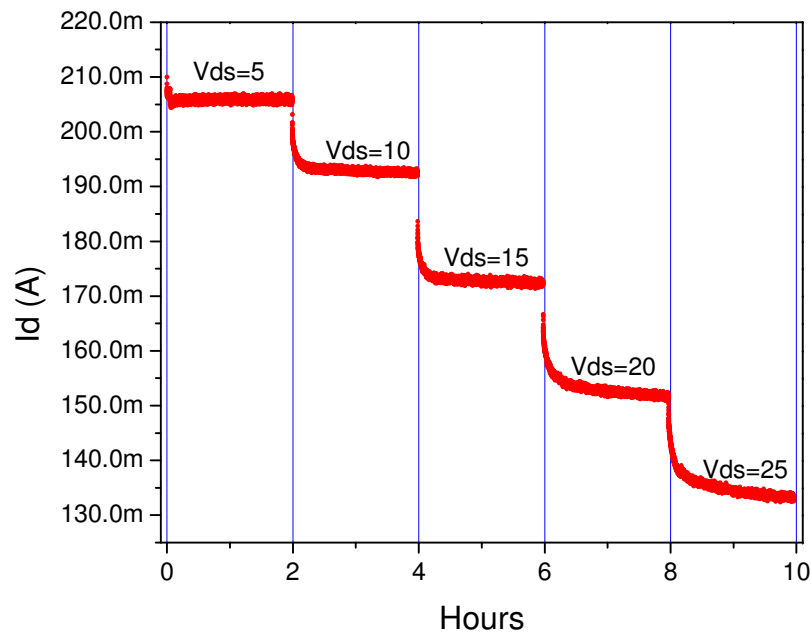
Implementation Pitfalls/Challenges

- Noise, Interference, Crosstalk
 - Shielded cable
 - Ground loop elimination
- Drain current sensing
 - High-side sensing: $V_S=0$ & $V_{GS}=V_G$
 - Foil resistors
 - Sense IC's
- DAQ Coordination
 - Simultaneous reads
 - Equipment sharing

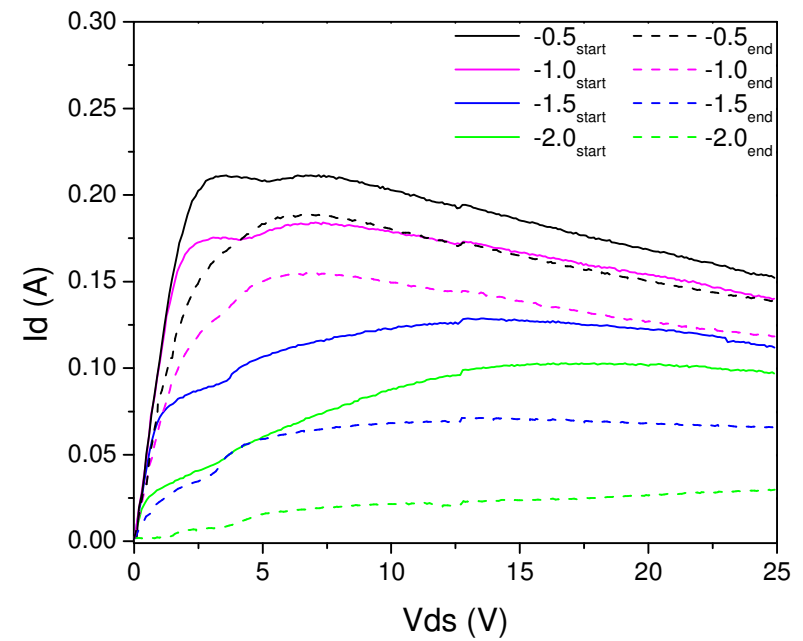
Data

GaN HEMT

Device 15

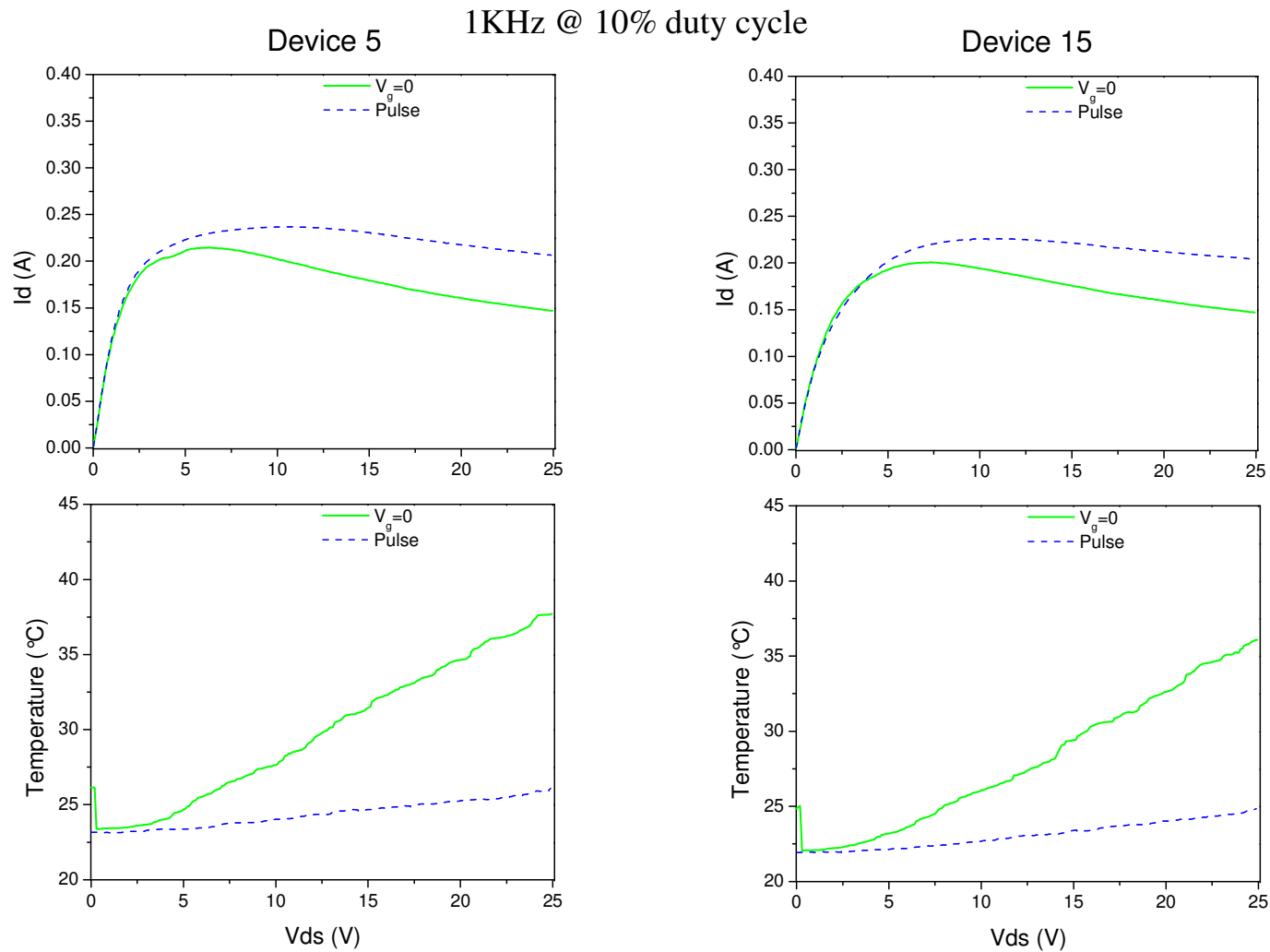


Device 15



Data

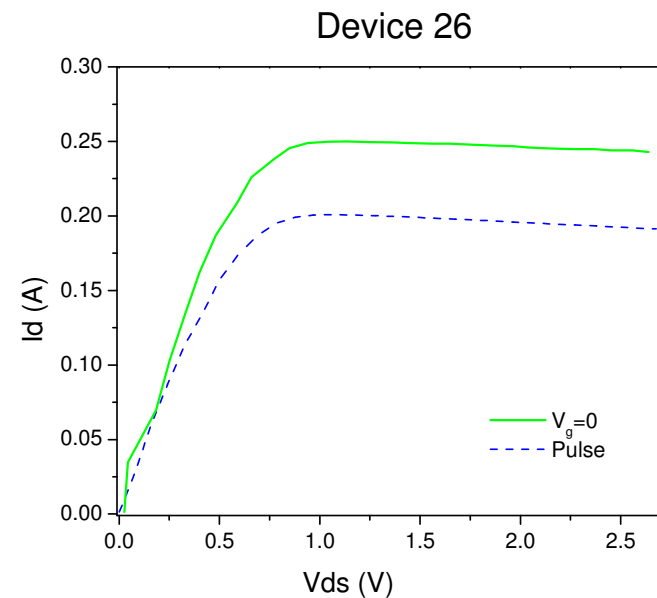
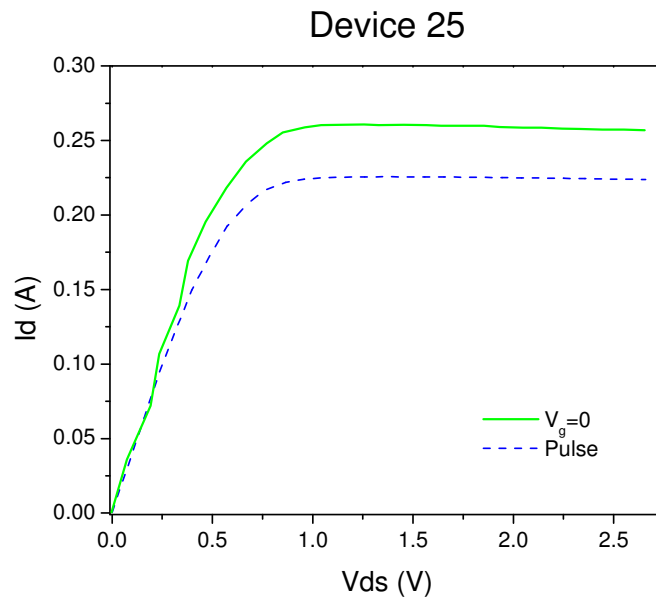
GaN Pulse Measurement



Data

GaAs Pulse Measurement

1KHz @ 10% duty cycle

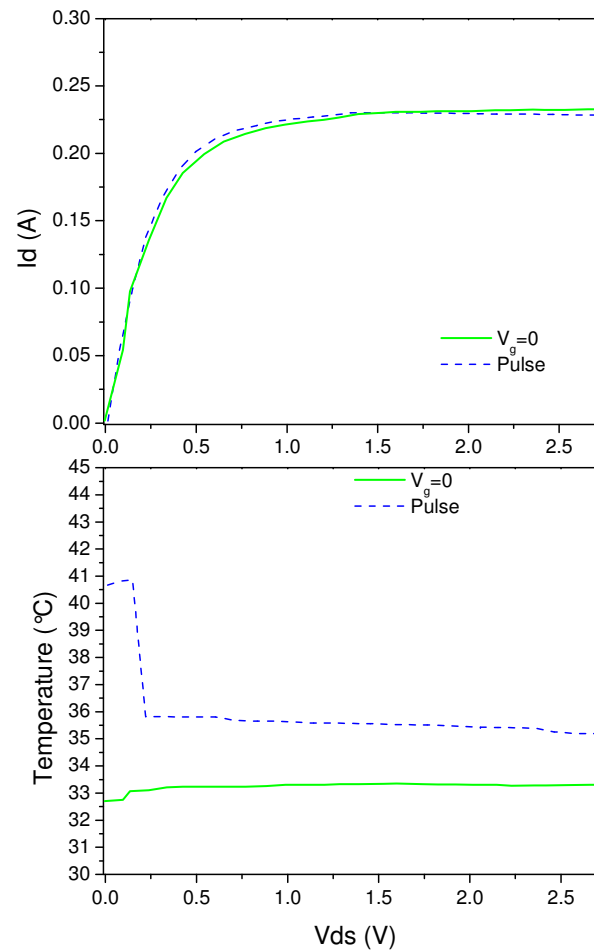


Data

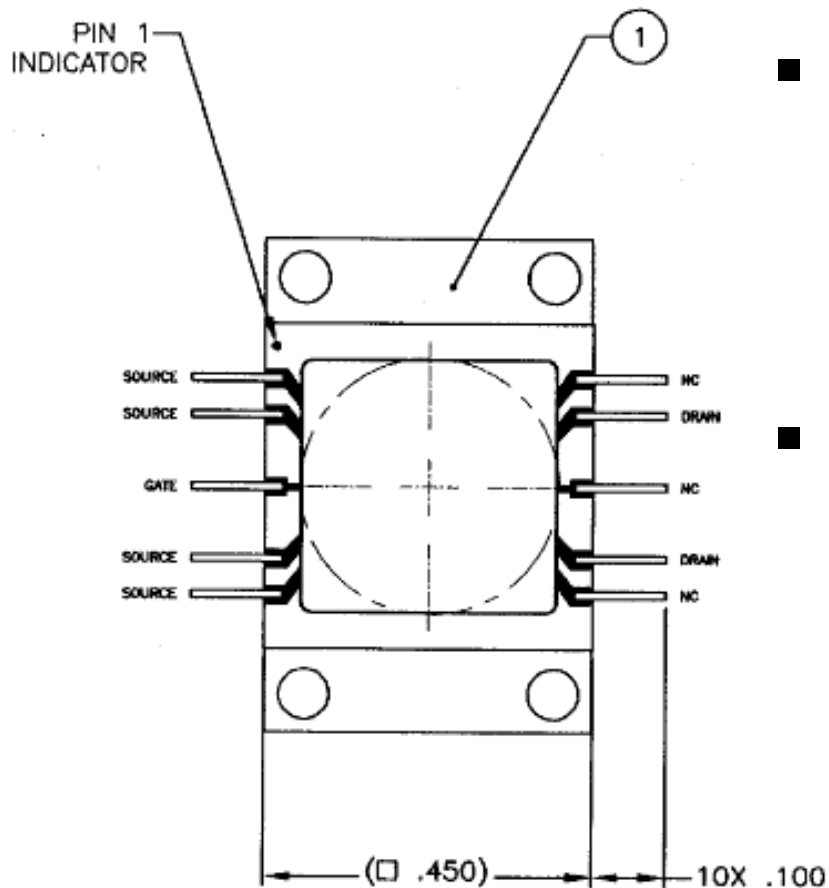
Si Pulse Measurement

1KHz @ 10% duty cycle

Device 24



AFRL Devices



- Packaging
 - 100 Devices at StatEdge
 - 25 from each subreticle A, B, C, & D
 - Delivery 1st week of October
- Test Strategy
 - Initial Drain step stress
 - Gate step stress
 - IV & Pulse testing to measure degradation

Future Work

- Prototypes to Production
 - PCB's
 - Populate and wire
- High speed pulse
- Optical pumping
- RF Integration